CONTACT PLUG PROCESSING AND A CONTACT PLUG

Field of the Invention

[0001] The invention relates to a semiconductor device having a contact hole formed by etching in a tapered fashion.

Background of the Invention

[0002] The increasing miniaturization of semiconductor devices has greatly reduced the size of contact holes, which are also referred to as via holes. The advent of 0.18 μm semiconductor processing has produced a myriad of problems such as shape defects caused by insufficient margin in the photolithography step. The etching process becomes increasingly difficult due to the reduced thickness of the photoresist that serves as mask material for etching. Changes in contact dimensions result from the variance of the thickness of interlayer insulation films.

[0003] The dielectric layer between the active devices in silicon and the first metal layer is termed the premetal dielectric (PMD). The PMD is also termed the first interlayer dielectric (ILD-1). The PMD is typically a doped silicon dioxide, or glass. An important function of the PMD layer is to isolate transistor devices in two ways: electrically from the metal interconnect layer, and physically from contamination sources such as mobile ions. The PMD has a restricted thermal budget in high-performance devices so as to minimize degrading the transistor's characteristics.

[0004] The ILD is an insulating material that electrically separates the metal levels in multilevel metallization. Once deposited, the ILD is patterned an etched to form via pathways for the various metal layers and the silicon. The via holes, also called contact holes, are filled with a metal, conventionally tungsten (W), to form the via hole plug. There are many via holes on a wafer, up to 10^{11} vias on each individual layer of a 300 mm product wafer. This process of creating via holes in the ILD is repeated for every ILD layer, including the PMD. In conventional metallization, a blanket layer of aluminum alloy metal is deposited on the dielectric layer, patterned and then etched to

form metal lines. The metal etch is an important technology in conventional metallization.

[0005] Figure 7 shows a semiconductor device having a via hole manufactured according to the conventional art. In Figure 7, a transistor has a silicon substrate 1 and a field area 2 that divides one transistor from another. Over the substrate a transistor gate 3 is formed. Over the transistor gate a silicon nitride (Si_3N_4) passivation layer 4 is formed. Alternatively, silicon oxynitride can be used to form a passivation layer. Over the silicon nitride passivation layer is deposited the BPSC (borophsophosilicate glass) or PMD (premetal dielectric). The materials that can be used for the PMD include FSG (silicon oxyfluoride), HSQ (hydrogen silsesquioxane), nanoporous silica, PAE (polyarylene ether), FLAC (fluorinated amorphous carbon) or AF4 (aliphatic tetrafluorinated poly-p-xylylene).

[0006] In the conventional art of Figure 7, an antireflective coating (ARC) 7 is provided directly on top of the PMD layer 5. Over the ARC 7 is formed a layer of photoresist 8 having openings over the portions where the via holes are to be formed. In the conventional art, a problem arises from the different lengths of the via holes, the via hole over the gate being shorter than the via hole over the source or drain. It is desirable that the via holes be cut straight. However, in the conventional art the photoresist has a wide opening over the via hole and the resulting via hole is tapered. As a result, the diameter l_1 of the via hole over the gate and the diameter of the via hole l_2 that is not over the gate is not equal so that $l_1 \neq l_2$.

[0007] Additional disadvantages associated with the conventional art is that the ARC layer is not completely opaque, and at least some light can penetrate through the ARC. When the phase of the incoming light wave and the phase of the reflective light wave are the same, the intensity of the light equals the sum of the intensities of both the incoming and reflective light. If the phase differs by 180 degrees, then the light cancels each other to cause extinction. The phase can be adjusted by adjusting

the thickness of the layer, so that the incoming and reflected light cancel each other.

[0008] The difficulty associated with adjusting the ARC layer arises from the subsequent requirement to etch the nitride layer. However, both the ARC and the nitride layer have similar etch characteristics, which means that they both etch at the same speed. As a result, the nitride layer does not act as a mask and the thickness of the ARC layer is difficult to control using the conventional technology.

[0009] Additional disadvantages of the conventional technology are associated with the treatment subsequent to opening the via holes. After opening the via hole, Ti and TiN are sputtered to reduce resistance at the contact. Afterwards, the contact hole is filled with tungsten. During the sputtering, Ti and TiN overhang the via hole. This occurs because the sputtering process causes the Ti and TiN to approach the via hole at an angle. As a result, Ti and TiN overhang the via hole to narrow the opening of the via hole. This overhang prevents the tungsten from properly filling the via hole. To prevent this improper filling, the opening can be tapered, but this taper would then result in the associated problem of the diameter of the via hole over the gate being different than the diameter of the via hole not over the gate. Therefore, tapering the via hole does not provide an ideal solution to reduce the disadvantages caused by the Ti and TiN overhang.

SUMMARY OF THE INVENTION

[0010] The invention, in part, provides a method for fabricating a semiconductor device that substantially eliminates one or more of the problems due to limitations and disadvantages of the related art.

[0011] The invention, in part, provides a method of creating a contact for a semiconductor device that entails depositing a PMD layer on the semiconductor device, depositing a silicon layer and an antireflection layer over the PMD layer, etching the silicon and antireflection layers in a tapered fashion, etching a via

hole in the PMD layer in a non-tapered fashion, and forming the contact in the etched via hole. The via holes can be lined with Ti/TiN . The via holes can be filled with tungsten, or the via holes can be lined with Ta/TaN and filled with copper. The contacts are formed from a metal that can be at least one of tungsten, copper, and copper alloy.

[0012] The invention, in part, pertains to a semiconductor device that has a substrate, at least one gate over the substrate, a PMD layer over the gate and the substrate, at least one via hole over the gate, and at least one via hole not over the gate, so that the via hole over the gate is not tapered and the via hole not over the gate is not tapered.

[0013] The invention, in part, pertains to the via hole over the gate and the via hole not over the gate both have the same diameter.

[0014] The invention, in part, pertains to via holes anisotropically formed through a PMD layer so that the via holes have parallel walls.

[0015] The invention, in part, pertains to a semiconductor device having via holes formed by depositing a silicon layer over the PMD layer, depositing an antireflective layer over the PMD layer, etching a tapered hole through the antireflective layer and the silicon layer, and anisotropically etching the PMD layer.

[0016] Advantages of the present invention will become more apparent from the detailed description given herein after. However, it should be understood that the detailed description and specific examples, while indicating preferred embodiments of the invention, are given by way of illustration only, since various changes and modifications within the spirit and scope of the invention will become apparent to those skilled in the art from this detailed description.

Brief Description of the Drawings

[0017] The accompanying drawings are included to provide a further understanding of the invention. The drawings illustrate embodiments of the invention and together with the description

serve to explain the principles of the embodiments of the invention.

[0018] Figure 1 is a diagram of a process to form a semiconductor via hole according to the invention.

[0019] Figure 2 shows the initial stage of the etch process to form the via hole.

[0020] Figure 3 shows the an anisotropic etch through the PMD layer.

[0021] Figure 4 shows a structural detail of Figure 3 highlighting the geometry of the via hole formation.

[0022] Figure 5 shows the application of the metal to the semiconductor.

[0023] Figure 6 shows the process following application of the metal fill.

[0024] Figure 7 shows a conventional art via hole technology.

Detailed Description

[0025] Advantages of the present invention will become more apparent from the detailed description given herein after. However, it should be understood that the detailed description and specific examples, while indicating preferred embodiments of the invention, are given by way of illustration only, since various changes and modifications within the spirit and scope of the invention will become apparent to those skilled in the art from this detailed description.

[0026] In order to solve the above-described problems associated with the conventional art, the invention, in part, deposits either amorphous silicon or polysilicon as a mask material and an organic or inorganic ARC after completing the formation of a gate electrode, SiN passivation layer deposition, interlayer film deposition, and flattening using CMP (chemical mechanical polishing).

[0027] By utilizing the two layers (silicon and ARC), the invention makes it possible to completely ignore dimensional changes caused by thickness variations of the films between base layers. Also, in order to improve the photo-process margin, a

regular taper was applied to the etching of interlayer films, and the resist pattern was made larger than the bottom diameter after contact formation. This alleviates such problems as the worsened dimensional variance caused by differences in the thickness of interlayer films on the active region, gate and other wafer surfaces. The invention minimizes short circuits between connection lines and other metal conductors formed on the upper part of the contact caused by an increase in the diameter of the opening in the upper part of the contact.

[0028] Figure 1 is a diagram of a process to form a semiconductor via hole according to the invention. A silicon substrate 1 has a field oxide film 2 formed in accordance with the conventional art. Gate electrode 3 is formed over the silicon substrate 1. A passivation layer 4 made of silicon nitride or silicon oxynitride is formed over the substrate 1, oxide film and gate 3. Above the passsivation layer 4 is deposed a PMD (also called ILD-1) layer 5. Over the PMD layer is first deposed a silicon layer 6 that can comprise either amorphous silicon or polycrystalline silicon. Over the silicon layer 6 is deposed an organic or inorganic ARC layer 7. Over the ARC layer 7, a photoresist layer 8 is formed having spaces over the portions where the via holes are to be formed.

[0029] The field oxide film 2 serves as an isolation barrier between individual transistors to isolate them from each other. Common field oxide film thickness ranges from about 2,500 Å to about 15,000 Å.

[0030] The gate electrode 3 can be formed by depositing a Poly-Si or a -Si or WSi on a SiO_2 or SiN film using a method such as CVD, and patterning the gate electrode 3 using photolithography and etching technology to form the gate electrode structure 3. The thickness of SiO_2 and SiN are less than 15nm. The thicknesses of Poly-Si, a-Si, and WSi are from 100nm to 300nm. The SiN is typically formed using LPCVD using a reaction of ammonia and dichlorosilane gas at a temperature of about 750°C or PCVD using a reaction of SiH_4 and NH_3 gas at a temperature of about 400°C.

[0031] The PMD 5 is deposited across the surface of the wafer using CVD, for example. The PMD is typically silicon dioxide, doped silicon dioxide or glass. The PMD can be borosilicate glass, PSG (phospohosilicate glass), BPSG (borophosphosilicate glass), or FSG (fluorosilicate glass, also call silicon oxyfluoride). Other materials suitable for the PMD HSQ (hydrogen silsesquioxane), nanoporous silica, PAE (polyarylene ether), FLAC (fluorinated amorphous carbon) or AF4 (aliphatic tetrafluorinated poly-p-xylylene).

[0032] The silicon layer 6 can be either amorphous silicon and polycrystalline silicon (polysilicon). The polysilicon can be deposed, for example, using silane gas in a LPCVD (low pressure chemical vapor deposition) furnace.

[0033] The ARC layer 7 reduces standing wave effects in the photoresist by applying an antireflective layer that suppresses unintended light reflection. The ARC layer 7 can include but are not restricted to SiO_2, Ta_2O_5, PMMA (polymethyl methacrylate) and polycarbonate. Water soluble polymers are frequently used to form ARCs. The ARC layer 7 can include, but are not restricted to, SiON, C, and organic ARC of ARS (Shipley Inc.).

[0034] The photoresist layer 8 can be a positive or negative photoresist. The positive photoresist can be, for example, a phenol-formaldehyde resin, also referred to as novolak. The photoresist can contain a sensitizer such as diazonaphthoquinone. The photoresist can be, for example, a chemically amplified photoresist containing an acid generator. The photoresist can be a DUV (deep ultraviolet) photoresist based on, for example, tert-butoxycarbonyl, polyhydroxy styrene, phenolic resin, or PMMA (polymethyl methacrylate). The photoresist can be diluted with a solvent such as EGMEA (ethyleneglycol monomethylether acetate) or PGMEA (propyleneglycol monomethylether acetate).

[0035] Figure 2 shows the initial stage of the etch process to form the via holes. A simple, regular taper is etched through the ARC layer 7 and the silicon layer 6. Typically Cl_2, HBr and O_2 gas are used to make taper profile, and the gas flow ratio is 1:3

to 5:0.1 and pressure is about 10mm Torr. Adjusting HBr flow ratio can control the taper angle.

[0036] Figure 3 shows the subsequent anisotropic etch through the PMD layer 5 and the passivation layer 4. The etch through the PMD layer 5 and the passivation layer 5 is performed so as to form a via hole having vertical walls as it passes through these layers. Typically C_5F_8, CO, O_2 and Ar gas are used to make a non taper profile of PMD layer 5, and the gas flow is 1:3:2:20 and pressure is about 15mm Torr. The O_2 gas flow ratio can control the taper angle. Then CH_2F_2, Ar and O_2 gas are used to etch layer 4, and the gas flow is 1:10:1 and pressure is about 50mm Torr.

[0037] Figure 4 shows a structural detail of Figure 3 highlighting the geometry of the via hole formation. The diameter of the via hole at the top surface of the ARC is designated by D, and the diameter of the via hole at the top of the PMD is designated by L. The diameter of the bottom of the via hole at the gate is designated by l_1. The diameter of the via hole that does not connect to the gate (that is, the via hole that extends to the substrate) is designated by l_2. In the embodiment of the invention shown in Figure 4, the diameter of the via hole at the top surface of the ARC, D, is greater than the diameter of the via hole at the top of the PMD, L, or $D > L$. The anisotropic etch through the PMD gives the via hole through the PMD vertical, untapered walls such that the via hole over the gate has $L = l_1$. Similarly, the via hole not over the gate has vertical, untapered wall such that $L = l_2$. As a result, the uniform wall geometry of the device gives $L = l_1 = l_2$. That is, the walls of the via holes through the PMD are parallel to each other.

[0038] After the via holes are formed, the via holes are filled with a metal 9, as is shown in Figure 5. The metal can be, but is not restricted to, tungsten, copper, and copper alloys. Copper is preferred for the 0.08 μm and more advanced technologies. In the via hole, a barrier metal such as Ti/TiN or Ta/TaN may be used.

[0039] As has been shown, the method for fabricating a semiconductor device according to the invention has the many

advantages. The metal fill 9 can be applied using a number of methods such as electrochemical deposition.

[0040] Figure 6 shows the process following application of the metal fill 9. The metal fill 9, the ARC 8 and the silicon layer 7 are removed in a damascene process using CMP (chemical mechanical planarization). This planarizes the surface and prepares for the next level of ILD. The resulting surface has a planar geometry with metal inlays in the PMD to form the circuitry.

[0041] The advantages of the invention include the ability to form an ARC layer whose thickness can be easily adjusted. As a result the light can be canceled so as not to affect the PMD layer. This advantage is especially critical such light sources as a krypton laser (λ = 248 nm) or an argon fluoride laser (λ = 193 nm) is used.

[0042] The anisotropic profile of the via holes made according to the invention is highly advantageous. Sputtered materials do not overhang the via hole to interfere with semiconductor processing, such as is observed with tapered via hole geometries. The invention additionally minimizes disadvantages arising from the changes in film thicknesses of the layers. This improved dimensional variance signifies a marked improvement over the conventional art.

[0043] The foregoing embodiments and advantages are merely exemplary and are not to be construed as limiting the present invention. The present teaching can be readily applied to other types of apparatuses. The description of the present invention is intended to be illustrative, and not to limit the scope of the claims. Many alternatives, modifications, and variations will be apparent to those skilled in the art. It is to be understood that the foregoing descriptions and specific embodiments shown herein are merely illustrative of the best mode of the invention and the principles thereof, which is therefore understood to be limited only by the scope of the appended claims.